Also, the dependency of claim 14 has been corrected, thereby also rendering the rejection of claim 14 under 35 USC 112, second paragraph, moot.

Finally, claims 11 and 17 have been amended so as to even more clearly patentably distinguish the present invention over USP 5,004,703 to Zdebel et al., USP 6,027,983 to Hashimoto et al., USP 5,536,675 to Bohr et al., USP 6,326, 310 to Chang et al., and USP 5,763,315 to Benedict et al.

An object of the present invention is to prevent an electric field from concentrating at the upper corners of a substrate where a trench of a trench isolation layer is formed. To this end, a thermal oxide layer is provided at the upper corners of the substrate, wherein the interface between the thermal oxide layer and the substrate is rounded.

In the embodiment of FIGS. 8 – 14, as set out in claim 11, a semiconductor substrate 104 is etched using a hard mask pattern 108 as a mask to form a shallow trench 112 (FIG. 9), a thermal oxide layer 114 is formed along opposed side walls and a bottom wall of the shallow trench, wherein the thermal oxide layer has **lateral portions each having a curvilinear sectional profile at an interface with the upper surface of the semiconductor substrate** (FIG. 10), and the resulting structure is etched using the hard mask pattern as a mask to extend the shallow trench deeper into the semiconductor substrate and leave the curved lateral portions of the thermal oxide in place (FIG. 11).

In the embodiment of FIGS. 15 and 16, as set forth in claim 17, the thermal oxide layer 214 is formed on a flat upper surface of the semiconductor substrate 204 between respective portions of the pad oxide pattern 206, wherein the thermal oxide layer has **lateral portions each having the sectional profile of a bird's beak** at an interface with the upper surface of the semiconductor substrate (FIG. 15), and the resulting structure is etched using the hard mask pattern 208 as a mask to thereby leave the lateral (bird's beak) portions of the thermal oxide at the interface with the upper surface of the semiconductor substrate.

Zdebel et al. does disclose a method of forming trench isolation structure in which a thermal oxide layer 26 is produced on the inner side walls of the substrate 10, 12, 14 that define the sides and bottom of a shallow trench 24 (*FIG.1*). However, unlike Applicants' invention of claim 11, the forming of the oxide layer 26 does not result in the lateral portions of the layer 26 having a curvilinear sectional profile at their interface with the substrate. Compare FIG. 1 of Zdebel et al. to FIG. 10 of the instant application. Thus, when the etching is carried out in Zdebel et al. to form deep trenches 34 (*FIG. 5*), the upper corners of the trenches 34 have a steep profile, like Applicants' admitted prior art (refer to p. 3, lines 4 – 7 of Applicants' original specification and FIG. 4), and unlike Applicants' invention of claim 11 (FIGS. 11 - 14).

The method disclosed by Zdebel et al. is likewise different form Applicants' method of claim 17. In particular, the forming of the oxide layer 26 in Zdebel et al. does not result in the lateral portions of the layer 26 having a bird's beak profile at their interface with the substrate. Compare FIG. 1 of Zdebel et al. to FIG. 15 of the instant application. Thus, when the etching is carried out in Zdebel et al. to form deep trenches 34 (*FIG. 5*), the upper corners of the trenches 34 have a steep profile, like Applicants' admitted prior art (refer to p. 3, lines 4 – 7 of Applicants' original specification and FIG. 4), and unlike the invention of claim 17 (FIG. 15).

Therefore, even assuming that one of ordinary skill in the art were motivated by the teachings of Hashimoto et al. to have filled the deep trenches 34 of Zdebel et al., to have planarized the resulting structure and to have removed the hard mask 18, 20 and 22, the result would still be different from Applicants' claims 11 and 17, as now amended. Such a result would still lack a method in which the thermal oxide layer formed at the upper corners of the trench provides a rounded interface with the substrate to prevent an electric field from concentrating at the upper corners.

The same comments essentially apply to the rejection relying on the primary reference to Bohr. Referring to FIGS. 3B and 3C of Bohr, although a thermal oxide layer 252a is formed in a shallow trench 242a, the lateral portions of

the thermal oxide layer 252a have neither a curvilinear sectional profile nor a bird's beak profile. Rather, the lateral portions of the thermal oxide layer 252a are formed to have a steep profile.

Applicants also respectfully submit that there is no suggestion which would have motivated one of ordinary skill in the art to have modified the method of Bohr in view of the teachings of Chang et al. "in order to control the trench profile" as suggested by the Examiner. First, Bohr already discloses an anisotropic etching that can control the profile of the deep trench 242b, if desired (col. 6, lines 15 – 19). Thus, there is no need or reason to turn to the teachings of Chang et al. Secondly, Chang et al. only suggest their method as a means of "providing shallow trench profile shaping". Thus, Chang et al. provide no suggestion that would have motivated one of ordinary skill in the art to have used their technique for forming the deep trench 242b of Bohr.

Nonetheless, even assuming *arguendo*, that one of ordinary skill in the art would have somehow been motivated by Chang et al. to have used side wall spacers in the method of forming the deep trench of Bohr, the result would still be different from each of claims 11 and 17 per the discussion above in connection with the Bohr reference.

The reference to Benedict et al. has also been reviewed but is not seen to overcome the deficiencies in the rejection based on the Zdebel et al. reference, as discussed above.

Finally, new claims 22 – 28 have been added so as to even further patentably distinguish the present invention over the prior art relied on by the Examiner.

For instance, new claims 23 and 24 set forth steps by which the method of the present invention forms a deep trench that has substantially the same width as the shallow trench (FIGS. 10 – 11). In both Zdebel et al. and Bohr, the deep trench is formed to be much narrower than the shallow trench. Similarly, new claim 26 specifies removing the entire portion of the thermal oxide layer that extends between the lateral portions having the sectional profile of a bird's beak (Figs. 15 – 16). On the other hand, the method of both Zdebel et al. and Bohr leave significant portions of the thermal oxide layer between respective portions of the pad oxide pattern when etching the deep trench.

Concerning new claims 25 and 28, Applicants first respectfully submit that Zdebel et al. do not disclose the forming of a buffer layer at all, contrary to the assertion made by the Examiner on page 4 of the Office Action. Rather, Zdebel et al. only disclose forming a trench liner (col. 3, lines 37 – 40). Note, Bohr only teaches growing an oxide layer 252b.

Regardless, neither Zdebel et al. nor Bohr teach a deposited oxide, i.e., an HTO oxide, an MTO oxide or a PE-oxide, as a buffer layer.

For these reasons, namely because of the above-described differences between Applicants' invention of claims 11 and 17 and the prior art references to Zdebel et al. and Bohr, it is seen that these references do not render Applicants' claims obvious under 35 USC 103. Accordingly, early reconsideration and allowance of the claims are respectfully requested.

Respectfully submitted,

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ATTACHMENT B

11. A method of manufacturing a trench isolation [~~structure of a semiconductor device~~] layer, the method comprising [~~the steps of~~]:

(a) sequentially forming a pad oxide layer and a hard mask layer on a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer by photolithography to form a hard mask pattern and a pad oxide pattern;

(c) etching a portion of the semiconductor substrate using the hard mask pattern as a mask to thereby form a shallow trench;

(d) forming a thermal oxide layer along inner walls of the semiconductor substrate that define opposed side walls and a bottom wall of the shallow trench, such that the thermal oxide layer has a central portion disposed along the inner wall of the substrate that defines the bottom of the shallow trench, and lateral portions disposed along the inner walls of the substrate that define the opposed side walls of the shallow trench, respectively, the lateral portions each having a curvilinear sectional profile at an interface with the upper surface of the semiconductor substrate;

(e) etching [~~away portions of the thermal oxide layer and the semiconductor substrate~~] the resulting structure using the hard mask pattern as a mask to extend said shallow trench deeper into the semiconductor substrate and thereby form a deep trench, wherein the central portion of the thermal oxide layer is removed, and the lateral portions of the thermal oxide are left in place;

(f) forming a buffer layer over the entire upper surface of the structure in which the deep trench has been formed;

(g) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(h) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(i) removing the hard mask pattern.

12. The method of claim 11, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and wherein step (c) comprises etching a portion of the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the shallow trench, and step (e) comprises etching the central portion of the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.

14. The method of claim [~~12~~] 13, and further comprising the step of forming a second oxide layer between the liner and the first oxide layer.

17. A method of manufacturing a trench isolation layer, the method comprising [~~the steps of~~]:

(a) sequentially forming a pad oxide layer and a hard mask layer on [an] a flat upper surface of a semiconductor substrate;

(b) patterning the hard mask layer and the pad oxide layer using photolithography to form a hard mask pattern and a pad oxide pattern on the flat upper surface of the semiconductor substrate;

(c) forming a thermal oxide layer on a portion of the flat upper surface of the semiconductor substrate [~~where a trench isolation layer will be formed~~] between respective portions of the pad oxide pattern, such that the thermal oxide layer has a central portion, and lateral portions each having the sectional profile of a bird's beak at an interface with the upper surface of the semiconductor substrate;

(d) etching [~~away portions of the thermal oxide layer and the semiconductor substrate~~] the resulting structure using the hard mask pattern as a mask to thereby form a deep trench, wherein the central portion of the thermal oxide layer is removed, and the lateral portions of the thermal oxide are left at the interface with the upper surface of the semiconductor substrate;

(e) forming a buffer layer over the entire upper surface of the resulting structure in which the deep trench has been formed;

(f) filling the deep trench, in which the buffer layer has been formed, with a first oxide layer;

(g) planarizing the resulting structure in which the deep trench has been filled with the first oxide layer; and

(h) removing the hard mask pattern.

18. The method of claim 17, and further comprising the step of forming a spacer along sidewalls of the hard mask pattern and the pad oxide pattern, and wherein

step (d) comprises etching the central portion of the thermal oxide layer and the semiconductor substrate using the hard mask pattern and the spacer as a mask to thereby form the deep trench.